

MUN5312DW1, NSBC124EPDXV6, NSBC124EPDP6

Complementary Bias Resistor Transistors R1 = 22 kΩ, R2 = 22 kΩ NPN and PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable*
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

(T_A = 25°C both polarities Q₁ (PNP) & Q₂ (NPN), unless otherwise noted)

Rating	Symbol	Max	Unit
Collector-Base Voltage	V _{CBO}	50	Vdc
Collector-Emitter Voltage	V _{CEO}	50	Vdc
Collector Current – Continuous	I _C	100	mAdc
Input Forward Voltage	V _{IN(fwd)}	40	Vdc
Input Reverse Voltage	V _{IN(rev)}	10	Vdc

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ORDERING INFORMATION

Device	Package	Shipping†
MUN5312DW1T1G, SMUN5312DW1T1G*	SOT-363	3,000 / Tape & Reel
NSVMUN5312DW1T3G*	SOT-363	10,000 / Tape & Reel
MUN5312DW1T2G, NSVMUN5312DW1T2G*	SOT-363	3,000 / Tape & Reel
NSBC124EPDXV6T1G	SOT-563	4,000 / Tape & Reel
NSBC124EPDXV6T5G	SOT-563	8,000 / Tape & Reel
NSBC124EPDP6T5G	SOT-963	8,000 / Tape & Reel

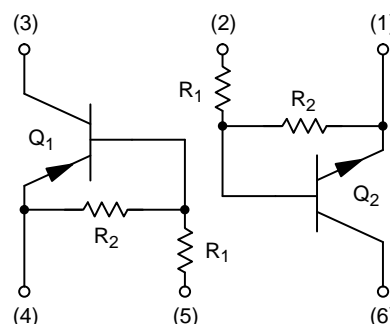
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



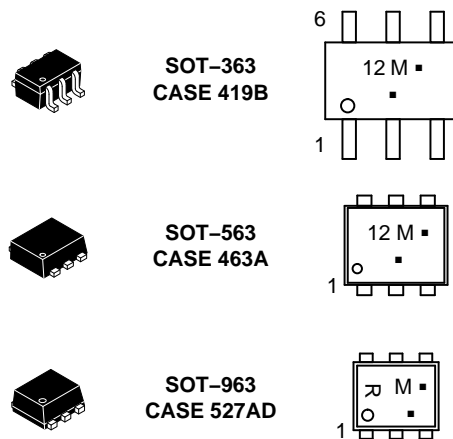
ON Semiconductor®

<http://onsemi.com>

PIN CONNECTIONS



MARKING DIAGRAMS



12/R = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

MUN5312DW1, NSBC124EPDXV6, NSBC124EPDP6

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
----------------	--------	-----	------

MUN5312DW1 (SOT-363) ONE JUNCTION HEATED

Total Device Dissipation $T_A = 25^\circ\text{C}$	(Note 1)	P_D	187	mW
	(Note 2)		256	
Derate above 25°C	(Note 1)		1.5	mW/ $^\circ\text{C}$
	(Note 2)		2.0	
Thermal Resistance, Junction to Ambient	(Note 1)	$R_{\theta JA}$	670	$^\circ\text{C/W}$
	(Note 2)		490	

MUN5312DW1 (SOT-363) BOTH JUNCTION HEATED (Note 3)

Total Device Dissipation $T_A = 25^\circ\text{C}$	(Note 1)	P_D	250	mW
	(Note 2)		385	
Derate above 25°C	(Note 1)		2.0	mW/ $^\circ\text{C}$
	(Note 2)		3.0	
Thermal Resistance, Junction to Ambient	(Note 1)	$R_{\theta JA}$	493	$^\circ\text{C/W}$
	(Note 2)		325	
Thermal Resistance, Junction to Lead	(Note 1)	$R_{\theta JL}$	188	$^\circ\text{C/W}$
	(Note 2)		208	
Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

NSBC124EPDXV6 (SOT-563) ONE JUNCTION HEATED

Total Device Dissipation $T_A = 25^\circ\text{C}$	(Note 1)	P_D	357	mW
Derate above 25°C	(Note 1)		2.9	mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	(Note 1)	$R_{\theta JA}$	350	$^\circ\text{C/W}$

NSBC124EPDXV6 (SOT-563) BOTH JUNCTION HEATED (Note 3)

Total Device Dissipation $T_A = 25^\circ\text{C}$	(Note 1)	P_D	500	mW
Derate above 25°C	(Note 1)		4.0	mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	(Note 1)	$R_{\theta JA}$	250	$^\circ\text{C/W}$
Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

NSBC124EPDP6 (SOT-963) ONE JUNCTION HEATED

Total Device Dissipation $T_A = 25^\circ\text{C}$	(Note 4)	P_D	231	MW
	(Note 5)		269	
Derate above 25°C	(Note 4)		1.9	mW/ $^\circ\text{C}$
	(Note 5)		2.2	
Thermal Resistance, Junction to Ambient	(Note 4)	$R_{\theta JA}$	540	$^\circ\text{C/W}$
	(Note 5)		464	

NSBC124EPDP6 (SOT-963) BOTH JUNCTION HEATED (Note 3)

Total Device Dissipation $T_A = 25^\circ\text{C}$	(Note 4)	P_D	339	MW
	(Note 5)		408	
Derate above 25°C	(Note 4)		2.7	mW/ $^\circ\text{C}$
	(Note 5)		3.3	
Thermal Resistance, Junction to Ambient	(Note 4)	$R_{\theta JA}$	369	$^\circ\text{C/W}$
	(Note 5)		306	
Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

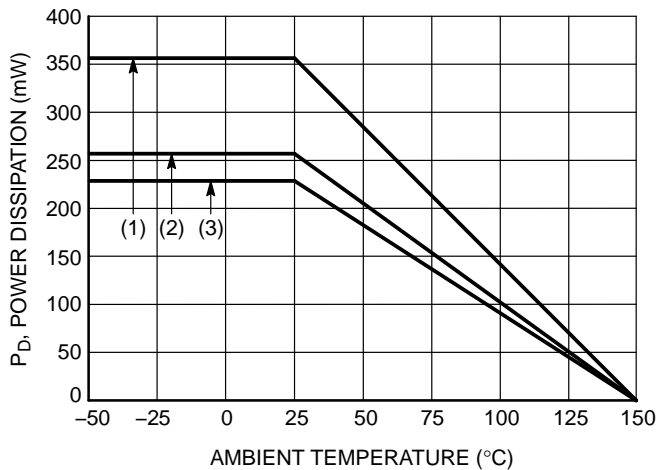
1. FR-4 @ Minimum Pad.
2. FR-4 @ 1.0×1.0 Inch Pad.
3. Both junction heated values assume total power is sum of two equally powered channels.
4. FR-4 @ 100 mm^2 , 1 oz. copper traces, still air.
5. FR-4 @ 500 mm^2 , 1 oz. copper traces, still air.

MUN5312DW1, NSBC124EPDXV6, NSBC124EPDP6

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ both polarities Q_1 (PNP) & Q_2 (NPN), unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Cutoff Current ($V_{CB} = 50\text{ V}$, $I_E = 0$)	I_{CBO}	-	-	100	nAdc
Collector-Emitter Cutoff Current ($V_{CE} = 50\text{ V}$, $I_B = 0$)	I_{CEO}	-	-	500	nAdc
Emitter-Base Cutoff Current ($V_{EB} = 6.0\text{ V}$, $I_C = 0$)	I_{EBO}	-	-	0.2	mAdc
Collector-Base Breakdown Voltage ($I_C = 10\ \mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	50	-	-	Vdc
Collector-Emitter Breakdown Voltage (Note 6) ($I_C = 2.0\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	50	-	-	Vdc
ON CHARACTERISTICS					
DC Current Gain (Note 6) ($I_C = 5.0\text{ mA}$, $V_{CE} = 10\text{ V}$)	h_{FE}	60	100	-	
Collector-Emitter Saturation Voltage (Note 6) ($I_C = 10\text{ mA}$, $I_B = 0.3\text{ mA}$)	$V_{CE(sat)}$	-	-	0.25	V
Input Voltage (Off) ($V_{CE} = 5.0\text{ V}$, $I_C = 100\ \mu\text{A}$) (NPN) ($V_{CE} = 5.0\text{ V}$, $I_C = 100\ \mu\text{A}$) (PNP)	$V_{i(off)}$	-	1.2	-	Vdc
Input Voltage (On) ($V_{CE} = 0.2\text{ V}$, $I_C = 5.0\text{ mA}$) (NPN) ($V_{CE} = 0.2\text{ V}$, $I_C = 5.0\text{ mA}$) (PNP)	$V_{i(on)}$	-	1.9	-	Vdc
Output Voltage (On) ($V_{CC} = 5.0\text{ V}$, $V_B = 2.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	V_{OL}	-	-	0.2	Vdc
Output Voltage (Off) ($V_{CC} = 5.0\text{ V}$, $V_B = 0.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	V_{OH}	4.9	-	-	Vdc
Input Resistor	R1	15.4	22	28.6	k Ω
Resistor Ratio	R_1/R_2	0.8	1.0	1.2	

6. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle \leq 2%.



- (1) SOT-363; 1.0 × 1.0 Inch Pad
- (2) SOT-563; Minimum Pad
- (3) SOT-963; 100 mm², 1 oz. Copper Trace

Figure 1. Derating Curve

TYPICAL CHARACTERISTICS – NPN TRANSISTOR
MUN5312DW1, NSBC124EPDXV6

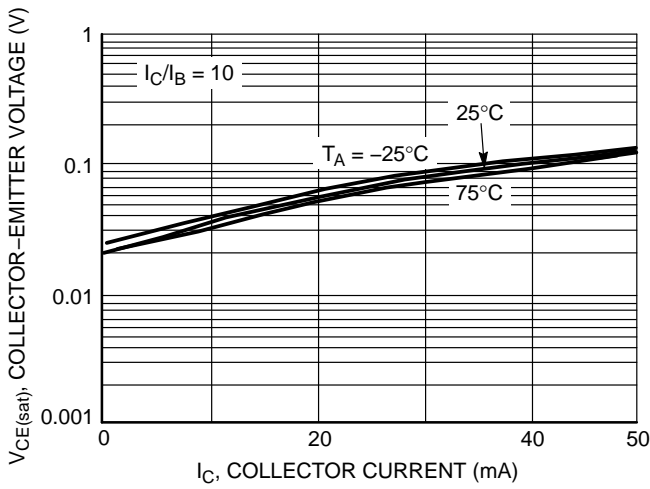


Figure 2. $V_{CE(sat)}$ vs. I_C

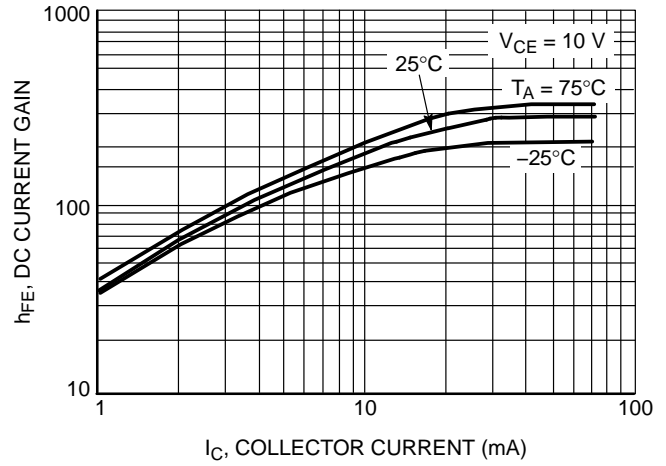


Figure 3. DC Current Gain

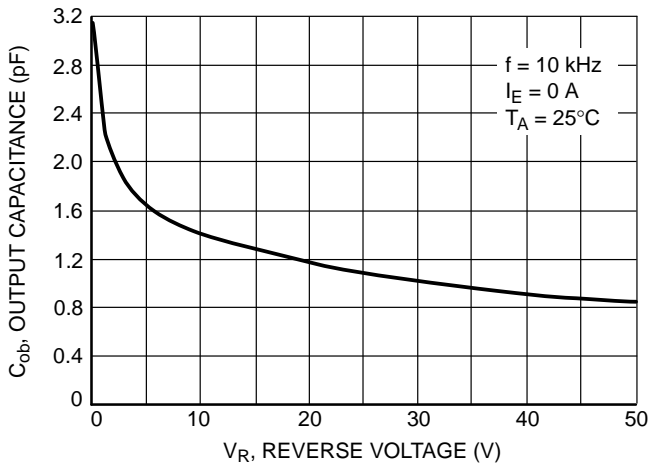


Figure 4. Output Capacitance

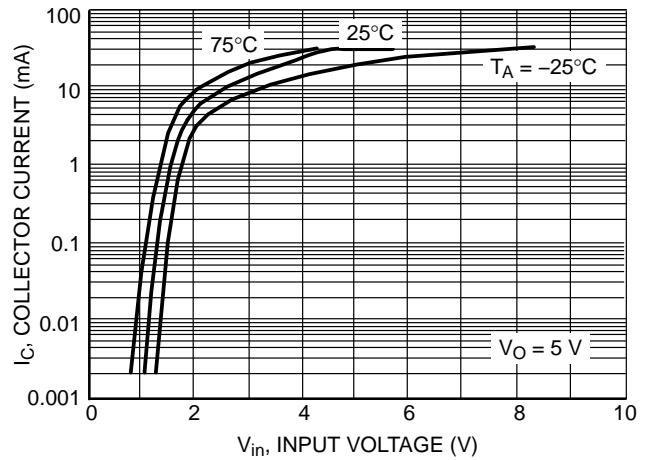


Figure 5. Output Current vs. Input Voltage

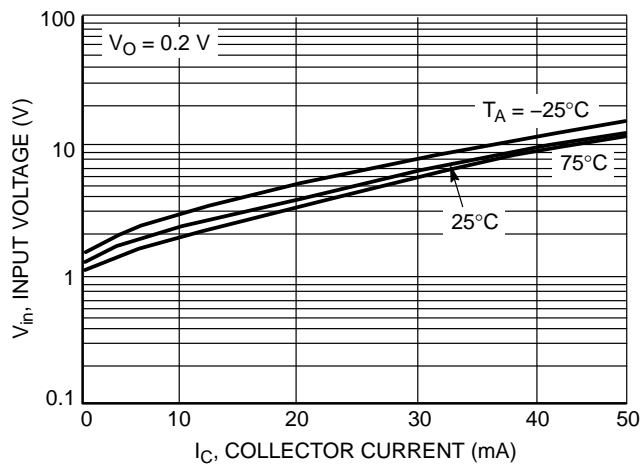


Figure 6. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS – PNP TRANSISTOR
MUN5312DW1, NSBC124EPDXV6

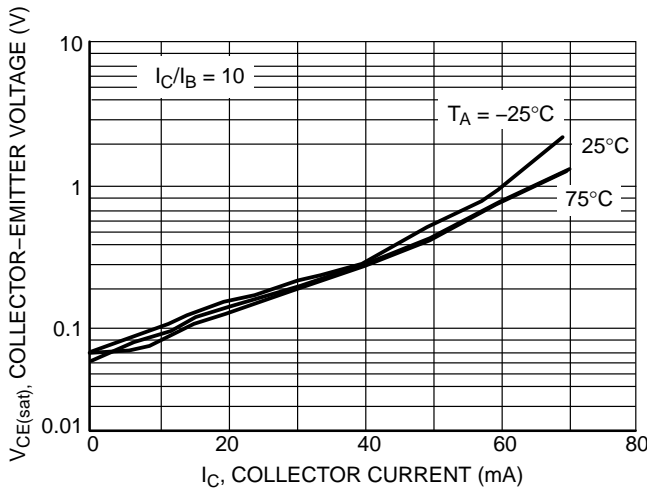


Figure 7. $V_{CE(sat)}$ vs. I_C

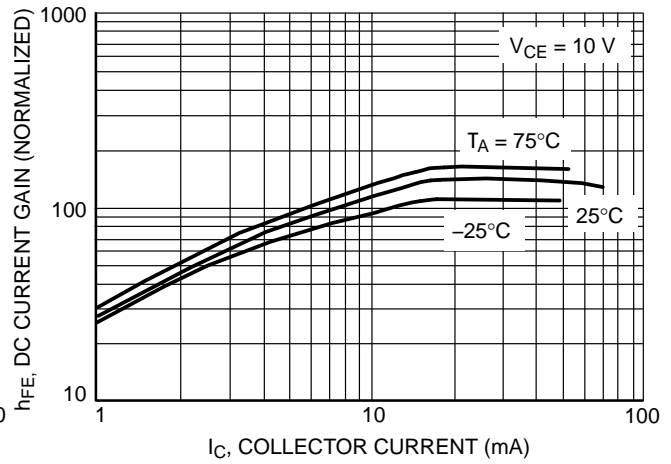


Figure 8. DC Current Gain

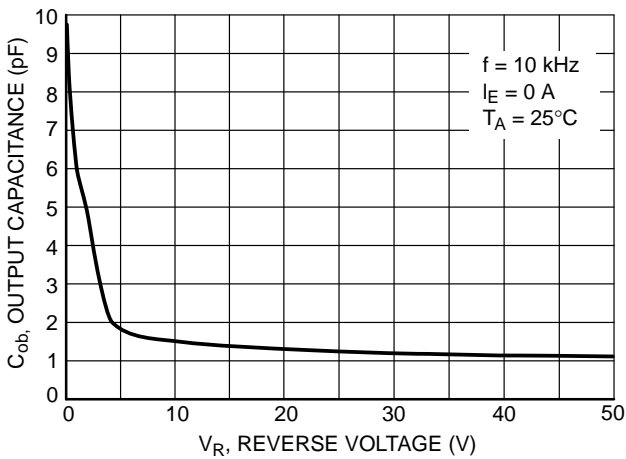


Figure 9. Output Capacitance

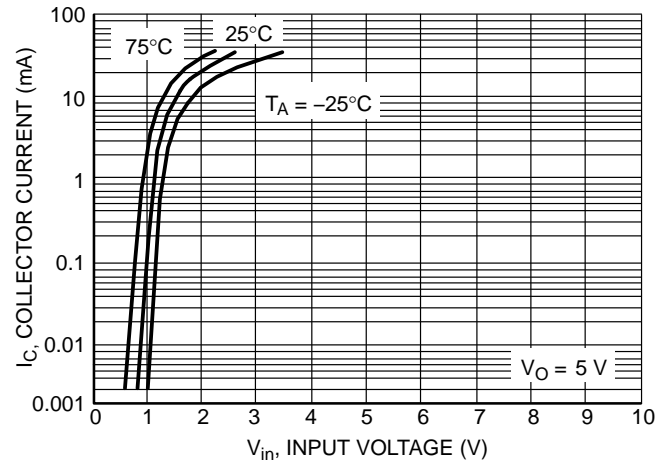


Figure 10. Output Current vs. Input Voltage

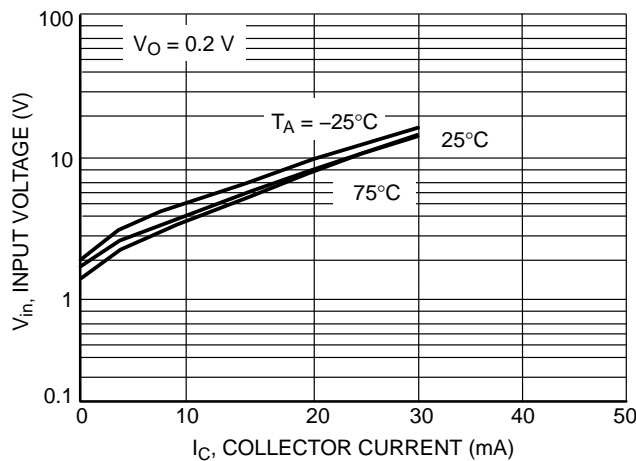


Figure 11. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS – NPN TRANSISTOR
NSBC124EPDP6

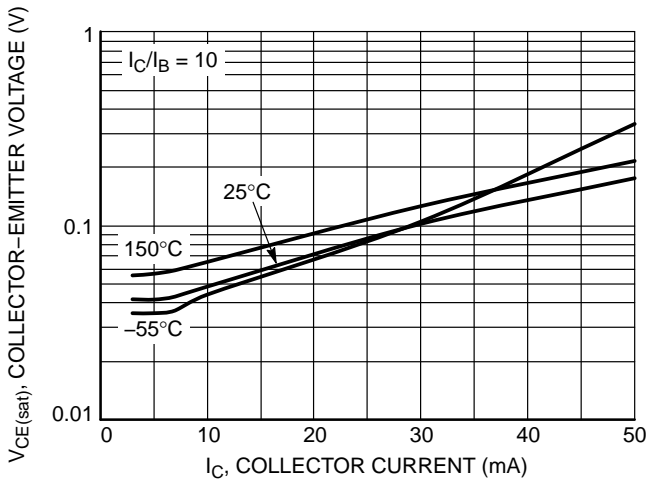


Figure 12. $V_{CE(sat)}$ vs. I_C

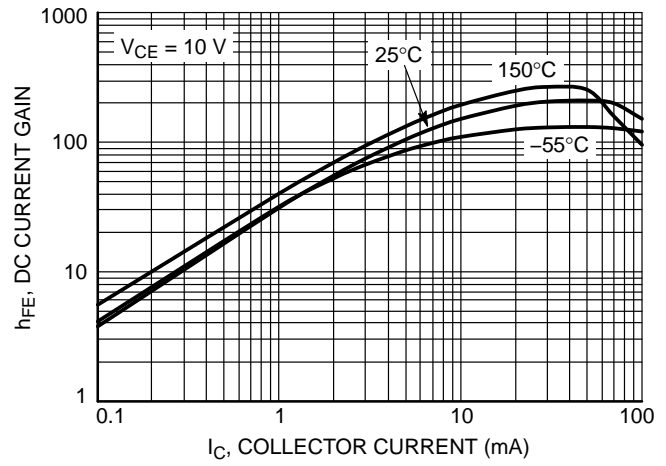


Figure 13. DC Current Gain

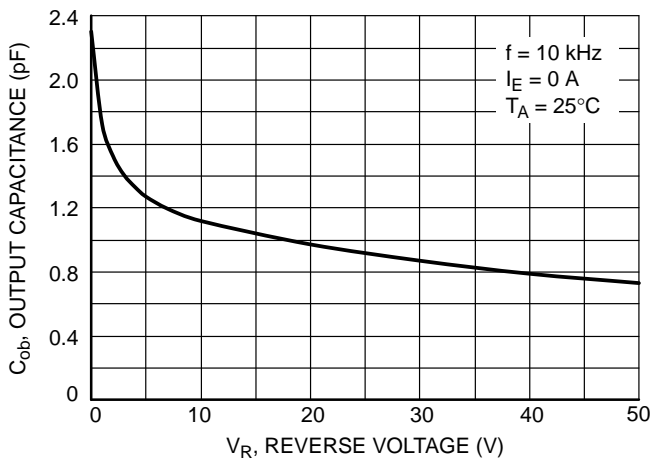


Figure 14. Output Capacitance

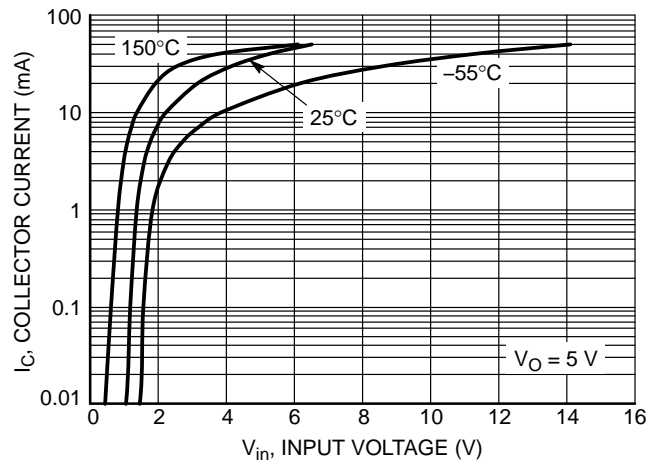


Figure 15. Output Current vs. Input Voltage

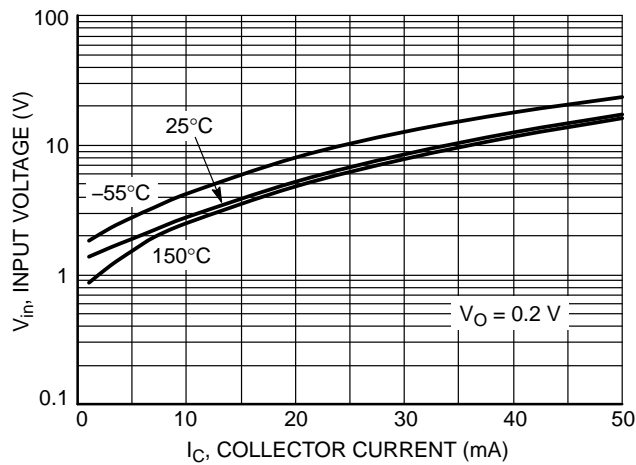


Figure 16. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS – PNP TRANSISTOR
NSBC124EPDP6

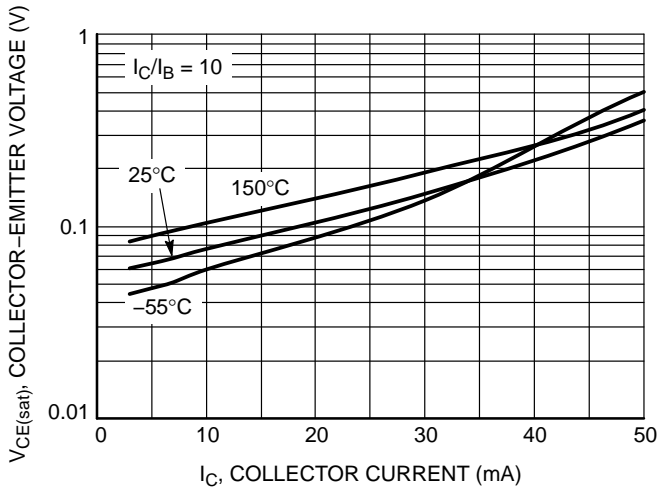


Figure 17. $V_{CE(sat)}$ vs. I_C

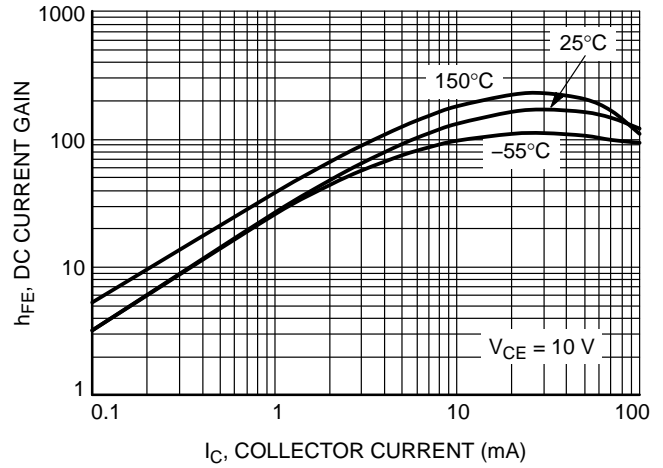


Figure 18. DC Current Gain

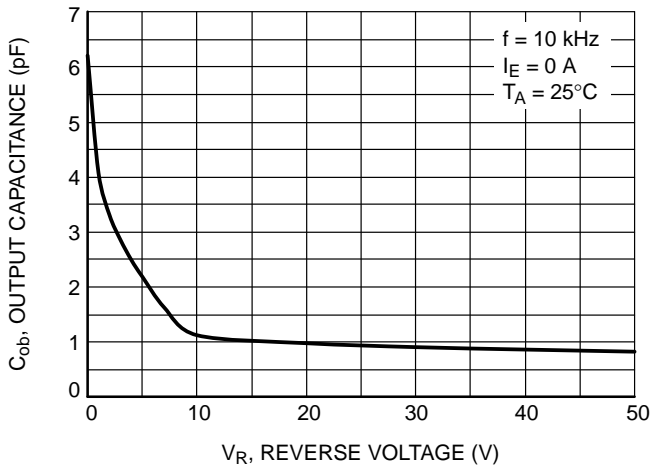


Figure 19. Output Capacitance

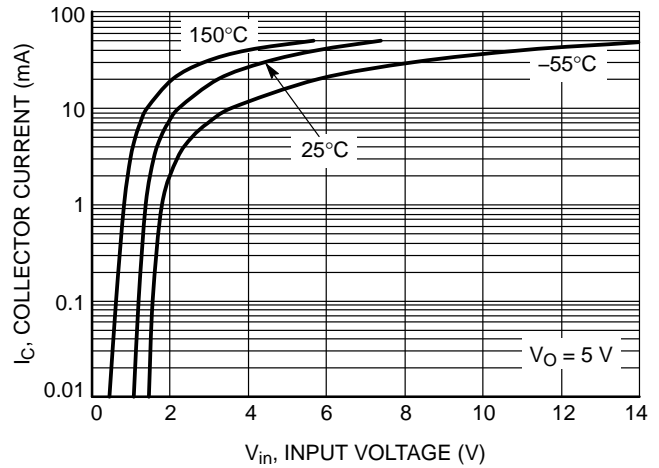


Figure 20. Output Current vs. Input Voltage

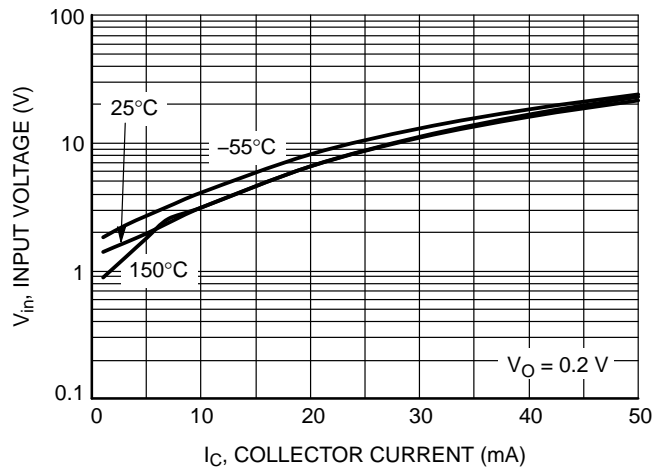
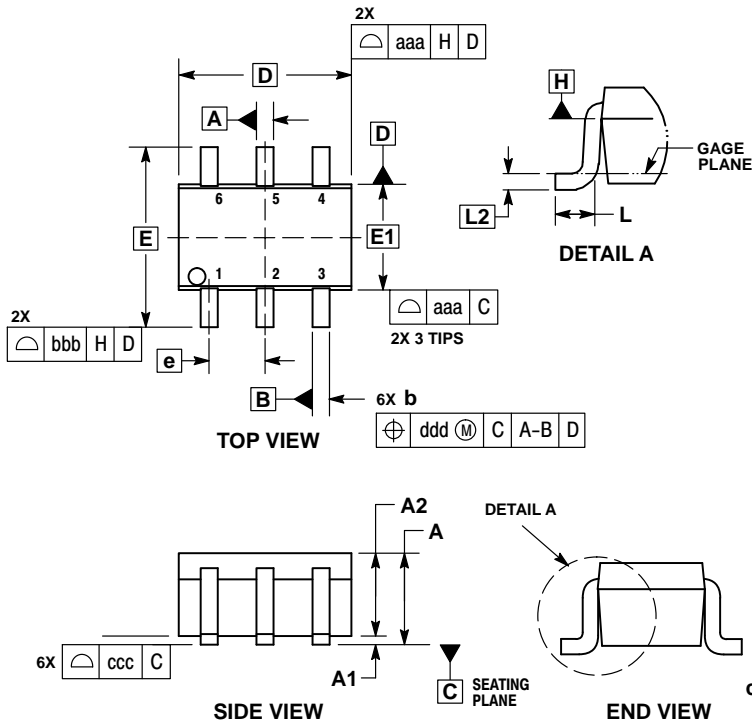


Figure 21. Input Voltage vs. Output Current

PACKAGE DIMENSIONS

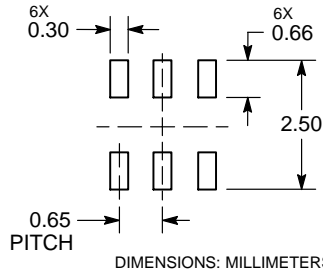
SC-88/SC70-6/SOT-363
 CASE 419B-02
 ISSUE Y



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
 4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
 5. DATUMS A AND B ARE DETERMINED AT DATUM H.
 6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
 7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

RECOMMENDED SOLDERING FOOTPRINT*

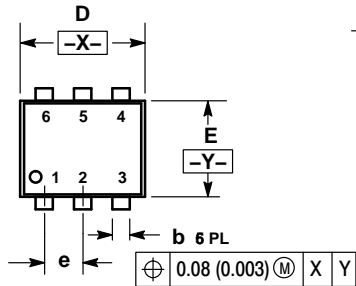


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MUN5312DW1, NSBC124EPDXV6, NSBC124EPDP6

PACKAGE DIMENSIONS

SOT-563, 6 LEAD
CASE 463A
ISSUE F

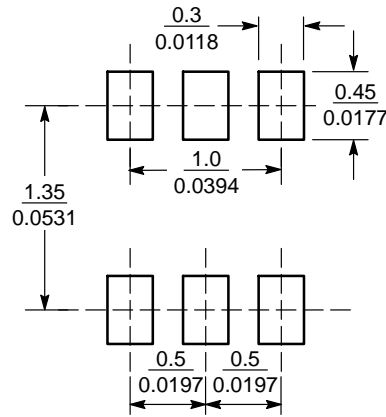


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.5 BSC			0.02 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H _E	1.50	1.60	1.70	0.059	0.062	0.066

SOLDERING FOOTPRINT*



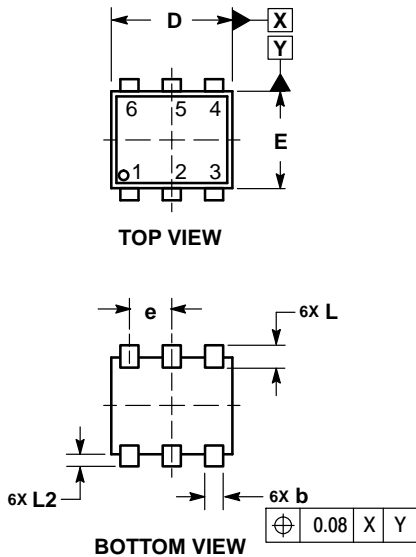
SCALE 20:1 ($\frac{\text{mm}}{\text{inches}}$)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MUN5312DW1, NSBC124EPDXV6, NSBC124EPDP6

PACKAGE DIMENSIONS

SOT-963 CASE 527AD ISSUE E

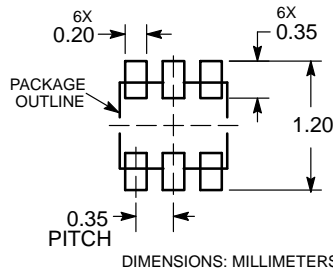


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H_E	0.95	1.00	1.05
L	0.19 REF		
L2	0.05	0.10	0.15

RECOMMENDED MOUNTING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative